

# Low Temperature Co-fired Multilayer Ceramic Substrates

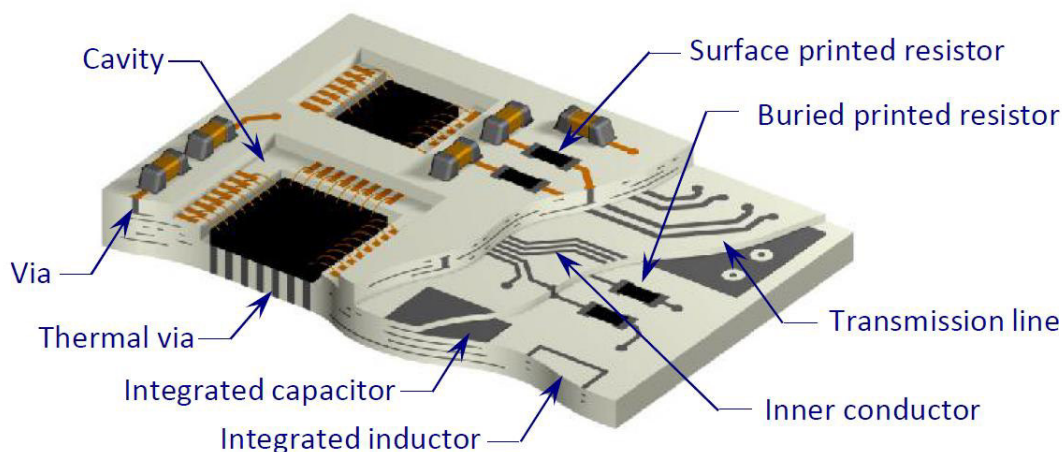


## Multilayer ceramics and cavity packages enable complex module creation

- Highly controlled dimensions, flatness**
- Ceramics with low dielectric constant & loss**
- Low thermal expansion enhances bare IC's use**
- Low ohm silver conductor**

**Optimal for bare chip module**

**High frequency performance**

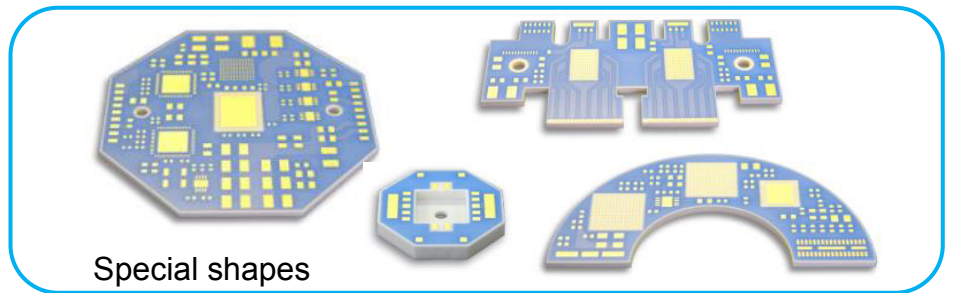
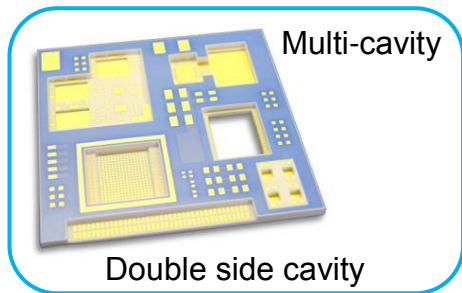
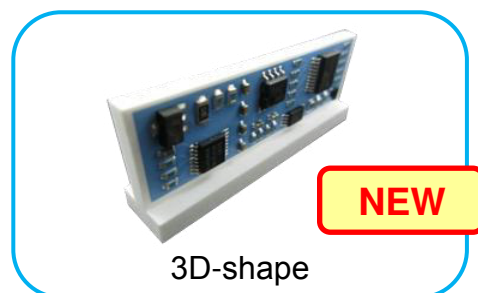
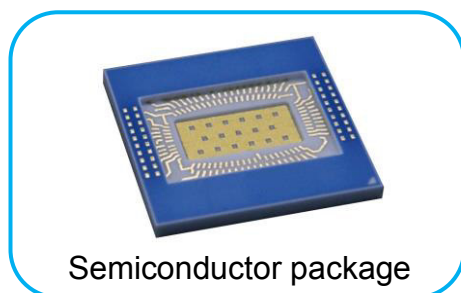
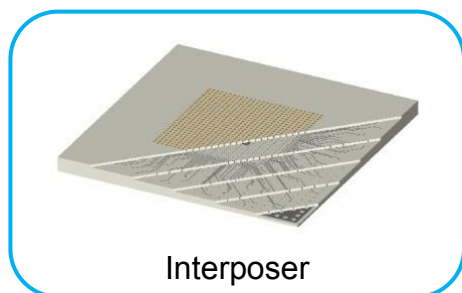


**Miniaturization & Integration**

**Environmental & reliability**

- Multilayer, multi & double side cavity**
- High heat/moisture resistance (zero water absorption)**
- Surface & buried printed resistors**
- Outgas/dust free, impermeability**

### Application Examples



For more information, please contact:  
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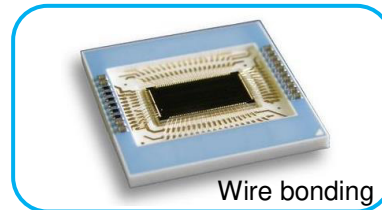
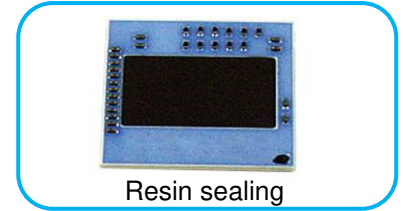
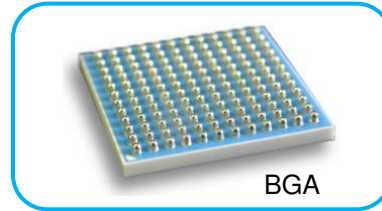
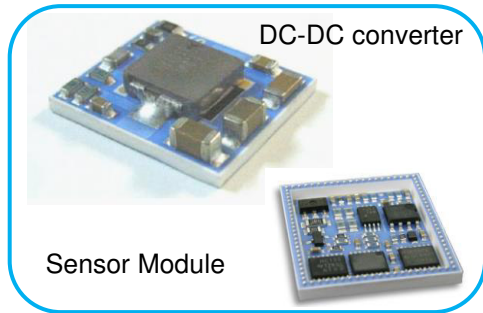
# Low Temperature Co-fired Multilayer Ceramic Substrates



## Pilot to Mass Production, Module Assembly

### Module Assembly

- Total support from design to assembly
- Reliability test on request



### High Flexibility

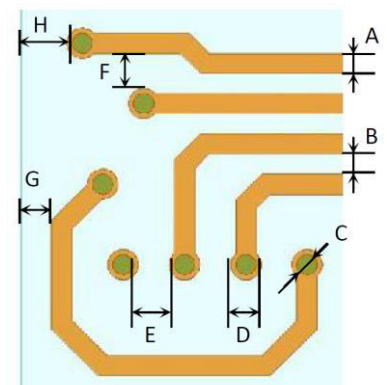
- Small to large volume production
- Low initial costs

## Material Characteristics

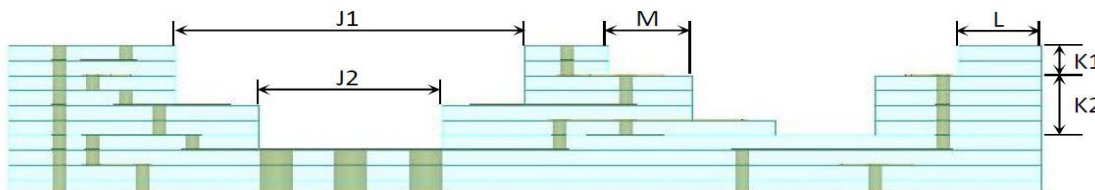
Parameter	Characteristics	
Bending strength	250	MPa
Thermal expansion coefficient	5.5	ppm / K
Thermal conductivity	3	W / m · K
Insulation resistance	$>10^{13}$	$\Omega \cdot \text{cm}$
Dielectric constant	6.8 (7)	at 75 GHz (1MHz)
Dielectric loss	$< 0.01$ (0.003)	at 75 GHz (1MHz)
Resistivity of buried conductor	Ag: 2.5	$\mu\Omega \cdot \text{cm}$
Density	2.8	$\text{g} / \text{cm}^3$
Surface roughness Ra	$< 0.4$	$\mu\text{m}$
Withstanding voltage	$> 15$	kV / mm
Layer thickness	80 / 100 / 125	$\mu\text{m}$

## Design Rules

Symbol	Parameter	Standard	Special
A	Line width	0.06 mm Min	0.05 mm Min
B	Line to line spacing	0.06 mm Min	0.05 mm Min
C	Via diameter	0.1 mm, 0.15 mm	0.06 mm Min
D	Via pad diameter	C + 0.05 mm Min	Pad less
E	Via to Via spacing	0.2 mm Min	0.08 mm Min
F	Via to line spacing	0.125 mm Min	0.075 mm Min
G	Part edge to conductor spacing	0.2 mm Min	0.10 mm Min
H	Part edge to Via pad spacing	0.3 mm Min	0.15 mm Min
J1, J2	Cavity width	0.6 mm Min	0.20 mm Min
K1, K2	Cavity depth	0.1 mm Min	0.08 mm Min
L	Cavity wall thickness	0.5 mm Min	-
M	Shelf width in the cavity	0.5 mm Min	0.01 mm Min



\* Please contact us for special design rules



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